Type: **EG1116/D EG9116C**

GaAs MONOLITHIC POWER AMPLIFIER 21.5 GHz TO 26.5 GHz

The EG1116 is a GaAs monolithic high-power amplifier that operates from 21.5 GHz -26.0 GHz. The amplifier is a one-stage device with two 1200um single-gate FET. It provides 7.0 dB typical small-signal gain and 29.5 dBm output power at 1-dB gain compression. The EG1116 is designed for use in Digital Multipoint as well as for Point to Point Radio Systems.

Bond pad and backside metallization is gold plated for compatibility with eutetic alloy attachment methods as well as the thermocompression and thermosonic wire bonding processes. Ground is provided to the circuitry through vias to the backside metallization.

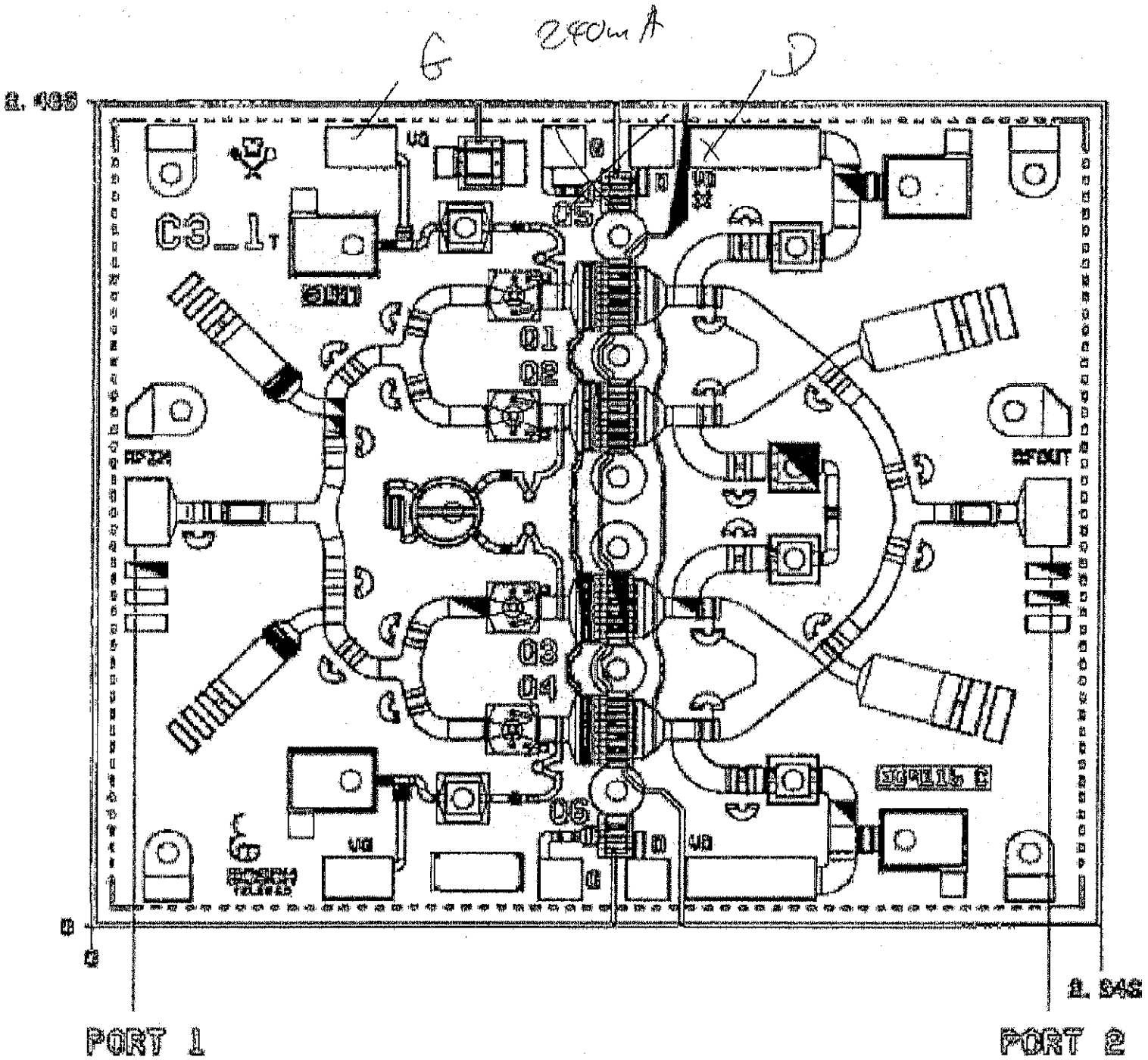
The MMIC is fabricated using a AlGaAs/GaAs 0.25 um T-gate PHEMT-Technology (Pseudomorphic High Electron Mobility Transistors) on an 100um thick GaAs substrate. For better DC & RF uniformity an "etch stop layer technique" for 1st and 2nd recess is applied.

,5

Chip Layout:Reference Planes/Ports for RF-Autoprobe

Chip Size:(2.946mm ± 50µm)x (2.489mm ± 50µm) X (0.1mm ± 12µm)

Port 1 RF Input Port 2 RF Output



1 Mounting, assembly and packaging

1.1 Semiconductor material :	GaAs
1.2 Bondpad metallization :	Au
1.3 Backside metallization :	Au
1.4 Chip mounting	
1.4.1 Adhesive, curing temperature :	Silver-filled epoxy, curing temperature < 200°C
1.4.2 Soldering :	with AuSn 20, fluxless, 320°C for 30 s
1.5 Bonding procedure :	Ball-TS
1.6 Bonding wire material and diameter :	Au 17 µm
1.7 Chip temperature during bonding :	< 200°C
1.8 Tool temperature during bonding :	< 200°C
1.9 Application :	Hybrid
1.10 Chip packaging method :	Wafflepack

1.2 Absolute Maximum Ratings

a) Chip thermal impedance is greatly affected by eutectic alloy attach methods and is approxin MMICs by measurements on discrete FETs.
b) Assumes equal current densities

1.3 Electrical Characteristics

ABSOLUTE MAX. RATINGS

T = +25 °C at heatsink

PARAMETER	**min.**	**max.**
V_{DS} drain source voltage	0.0	7.0 V |V_{DS}| + | V_{GS} | 8.0 V
V_{GS} gate source voltage	-5.0	0.0 V |V_{DS}| + | V_{GS} | 8.0 V
I_{DS} Drain-Source current	774 mA	
I_{BD} gate-to-drain breakdown current	2.4 mA	
$I_{Gate,max}$ Maximum allowable Gate Current	35.2 mA Strongly depends on P_{RF-IN}.	
P_{tot} Power dissipation	2.52 W	
P_{In} Input continuous wave power	27 dBm	
T_M Mounting temperature	320 °C max. 30 sec.	
T_B Bonding Temperature	200 °C	
T_{STG} Storage temperature	-65 150 °C	
T_{CH} Operating channel temperature	150 °C	
$THETA_{CH-B}$ Chip thermal impedance[a),b)] channel to backside	24 °C/W typical value	

Remark:
MTTF strongly depends on V_{DS} and channel temperature. Keep V_{DS} as low as possible.

RF-CHARACTERISTICS:

- Operating frequency band:	**21.5 GHz -26.5 GHz**
- Input / Output Ports:	**Z_0 = 50 Ω**
- Bias Condition:	**U_{DS} = 6.5 V ; I_{DS} = 240 mA**
S_{11} Input reflection loss	**-5.0 dB**
S_{22} Output reflection loss	**-5.0 dB**
S_{21} Small signal gain	**5.0 - 7.0 dB**
S_{12} Reverse isolation	**-35.0 dB**
P_{1dB} Output power at 1dB gain compressed	**28 - 29.5 dBm**

Chip Layout:Reference Planes/Ports for RF-Autoprobe

Chip Size:(2.946mm ± 50µm)x (2.489mm ± 50µm) X (0.1mm ± 12µm)

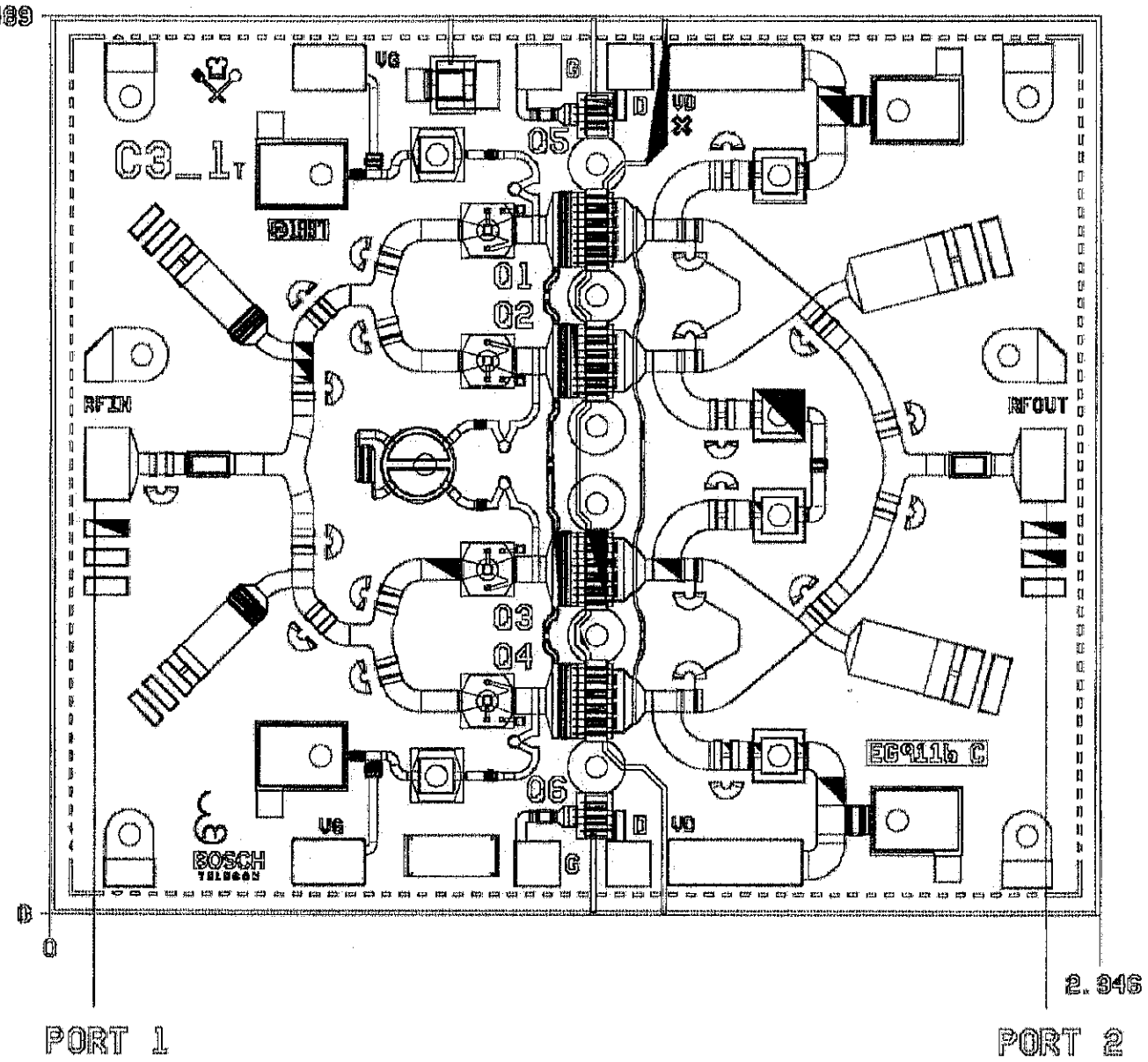


Fig.1

Port 1 RF Input Port 2 RF Output

Remarks: - RF autoprobe performed using TRL calibration technique for S-parameter

- GS, SG prober with 250µm pitch are used
- DC biasing performed using DC probe cards
- Reference Planes at center of TRL thru (914.4µm)

Distance from chip edge to the Saw/Scribe Marker Ticks (see Fig. 2). The nominal value for all four sides is d = 52.5 µm.

Top:	d = 52.5 µm ± 50 µm	Bottom:	d = 52.5 mm ± 50µm
Left:	d = 52.5 µm ± 25 µm	Right:	d = 52.5 mm ± 25µm

Capacitors to be checked for shortage:As much as possible.

1) $g_m=(I_{DSS} - I_{DS1})/(V_{GS}(I_{DSS}) - V_{GS1}(I_{DS1}))$ for $V_{DS}=V_{DSP}$

$V_{GS}(I_{DSS})=0V$, $V_{GS1}(I_{DS1})=-0.25V$,

$I_{DSS}=I_{DS}(V_{GS}=0V)$ for V_{DSP}

V_{DS} is swept between 0.5V and V_{DSP} in search of the maximum value of I_{DS}.

This maximum I_{DS} is recorded as I_{DS1}.

V_{DSP} is the drain voltage resulting in maximum

I_D for $V_{GS}=0V$, up to a maximum of 3.5V (also the point at which I_{DSS} is recorded).

RF-Autoprobe:

- Input / Output Ports: $Z_0 = 50\ \Omega$
- GS- or SG-RF-Autoprobes / 250 µm Pitch
- T = +25 °C at heatsink
- Reference planes as defined in Fig.1
- Measurement frequencies in GHz: 21.5, 23.0, 24.5, 26.5

- Bias Condition for RF- Autoprobe: $U_{DS} = 6.5\ V$; $I_{DS} = 240\ mA$

PARAMETER	min.	typ.	max.	Unit	Remarks
S_{11} Input reflection loss		-5.0		dB	**Info only**
S_{22} Output reflection loss		-5.0		dB	**Info only**
S_{21} Small signal gain	5.0	7.0		dB	
S_{12} Reverse isolation		-35.0		dB	**Info only**
P_{1dB} Output power at 1dB gain compressed	28	29.5		dBm	
RF-Autoprobe frequency points for IMD_3	23.0, 26.0			GHz	2 Test Frequencies
IMD_3 Intermodulation product 3rd order, f = 10 MHz		36		dBc	3 Input Power Levels **Info only** See note 1)

1) Measurements are made at 3 different input power levels. The input power levels (per tone) are calculated as followed (power levels rounded up to 0.5 dB):

P_{IN1} = 17dBm - Mean (S_{21} (dB) over the lot)

$P_{IN2,3} = P_{IN1} \pm 2dB$

1.2 Absolute Maximum Ratings

ABSOLUTE MAX. RATINGS T = +25 °C at heatsink				
PARAMETER	**min.**	**max.**	**Unit**	**Remarks**
V_{DS} drain source voltage	0.0	7.0	V	$\|V_{DS}\| + \|V_{GS}\|$ 8.0 V
V_{GS} gate source voltage	-5.0	0.0	V	$\|V_{DS}\| + \|V_{GS}\|$ 8.0 V
I_{DS} Drain-Source current		774	mA	
I_{BD} gate-to-drain breakdown current		2.4	mA	
$I_{Gate,max}$ Maximum allowable Gate Current		35.2	mA	Strongly depends on P_{RF-IN} .
P_{tot} Power dissipation		2.52	W	
P_{In} Input continuous wave power		27	dBm	
T_M Mounting temperature		320	°C	max. 30 sec.
T_B Bonding Temperature		200	°C	
T_{STG} Storage temperature	-65	150	°C	
T_{CH} Operating channel temperature		150	°C	
$THETA_{CH-B}$ Chip thermal impedance[a),b)] channel to backside	24		°C/W	typical value
Remark: MTTF strongly depends on V_{DS} and channel temperature. Keep V_{DS} as low as possible.				

a) Chip thermal impedance is greatly affected by eutectic alloy attach methods and is approximated for MMICs by measurements on discrete FETs.

b) Assumes equal current densities

1.3 Electrical Characteristics

DC-Autoprobe:

- Q1,2 & Q3,4 measured for total DC-Information (V_{BDGD}, V_{BDGS}, g_m, I_{DSS}, I_{MAX}, V_P)

-Q5 & Q6 measured for g_m, I_{DSS}, I_{MAX}, V_P

- T = +25 °C at heatsink

PARAMETER	**min.**	**typ.**	**max.**	**Unit**	**Remarks**
V_{BDGD} Breakdown voltage gate drain diode	-30.0	-21.0	-8.0	V	I_{BD} = 1.2mA per FET pair
V_{BDGS} Breakdown voltage gate source diode	-30.0	-21.0	-8.0	V	I_{BD} = 1.2mA per FET pair
g_m	264	450	636	mS	per FET pair see note 1)
I_{DSS} Drain Source Current for V_{GS}=0V		**Info**		mA	V_{DS}=6.5V No Sweep / Fix V_{DS}
I_{max} Maximum I_{DS}	450	612	774	mA	Positive voltage is applied to the gate to saturate the device. V_{DS} is stepped between 0.5 V up to a maximum of 3.5 V, searching for the maximum value of I_{DS}. Values are given per FET pair.
V_P Pinch--off voltage	-1.5	-1.0	-0.5	V	V_{DS} fixed at 2.0 V, V_{GS} is swept to bring I_{DS} to 0.6mA for FET pairs Q1,2 and Q3,4 and 0.09mA for FETs Q5 and Q6

2. Electrical Features

RF-CHARACTERISTICS:

- Operating frequency band: 21.5 GHz -26.5 GHz
- Input / Output Ports: Z_0 = 50 Ω
- GS- or SG-RF-Autoprobes / 250 µm Pitch
- T = +25 °C at heatsink
- Reference planes as defined in Fig.1

- Bias Condition: U_{DS} = 6.5 V ; I_{DS} = 240 mA

PARAMETER	typ.	Unit	Remarks
S_{11} Input reflection loss	-5.0	dB	
S_{22} Output reflection loss	-5.0	dB	
S_{21} Small signal gain	7.0	dB	
S_{12} Reverse isolation	-35.0	dB	
P_{1dB} Output power at 1dB gain compressed	29.5	dBm	
IMD_3 Intermodulation product 3rd order	36	dBc	Output Power Level P_{out} = 2 x 17 dBm, Δf = 10MHz

2.1 Marking and Packaging

Packing Devices into waffle packs:

1. The dies must be packed into the waffle packs as shown in Fig.3
2. Packing ist started with the lowest row & column number and continued increasing first the column number until the last die in this row. After finishing the row, row number is increased by one and the dies are picked starting with the last die in the new row. After picking the first die in this row, row number is increased again by one and picking is started at the first column; and so on.
3. The waffle pack is filled starting on the top left corner in the same way as the dies are picked from the wafer (see Fig. 4: Sorting dies into waffle pack).